Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) An electronic device for the recording/reproduction of voice data, comprising:

a chip of semiconductor material;

a main transmission line integrated in said chip;

a control unit integrated in said chip and connected to said main transmission line, the control unit being structured to provide a user interface to a user via an external user interface device;

a signal-conversion unit integrated in said chip and connected to said main transmission line, said signal-conversion unit comprising:

reception means for receiving an input analog signal correlated to a voice signal,

compression means for compressing said input analog signal and generating a first stream of compressed digital signals,

fetching means for receiving a second stream of compressed digital signals, and

decompression means for decompressing said second stream of compressed digital signals and generating an output analog signal;

a non-volatile memory unit integrated in said chip and connected to said main transmission line, said non-volatile memory unit storing said first stream of compressed digital data in memory locations, and generating said second stream of compressed digital signals according to first control signals generated by said control unit; and

a memory unit interface integrated in said chip and coupled between the non-volatile memory unit and said main transmission line, the memory unit interface being structured

to coordinate exchange of data and instructions between the non-volatile memory unit and said main transmission line.

2. (Original) The device according to claim 1 wherein said control unit further comprises a microprocessor.

3. (Original) The device according to claim 1 wherein said control unit further comprises a microcontroller.

4. (Original) The device according to claim 1 wherein said signal-conversion unit further comprises:

a converter circuit connected to said reception means; and

temporary-storage means coupled to said converter circuit for temporarily storing said first stream and said second stream of compressed digital signals.

5. (Previously Presented) The device according to claim 4 wherein said converter circuit further comprises dividing means for generating blocks of digital signals having a fixed dimension, each said block of digital signals comprising one portion of a pre-set duration of said voice signal.

6. (Previously Presented) The device according to claim 5 wherein said temporary-storage means further comprises a first memory buffer and a second memory buffer, and said signal-conversion unit further comprises control means for controlling transfer of said blocks of digital signals alternately to said first memory buffer and said second memory buffer according to second control signals supplied by said control unit.

7. (Original) The device according to claim 6 wherein said first and second memory buffers each further comprise a RAM type memory buffer.

8. (Previously Presented) The device according to claim 6 wherein said control means further comprises:

means for transferring first blocks of the first stream of compressed digital signals to said first memory buffer;

first means for detecting filling of said first memory buffer;

first transfer-switching means for transferring second blocks of the first stream of compressed digital signals to said second memory buffer and for sending said first blocks of digital signals to said non-volatile memory unit;

second means for detecting filling of said second memory buffer; and

second transfer-switching means for transferring third blocks of the first stream of compressed digital signals to said first memory buffer and for sending said second blocks of digital signals to said non-volatile memory unit.

9. (Original) The device according to claim 1 wherein said non-volatile memory unit further comprises a memory device having:

a first memory area storing said first stream of digital signals in said memory locations; and

a second memory area storing information regarding occupation of said memory locations of said first memory area.

10. (Original) The device according to claim 9 wherein said second memory area further comprises a first sub-area and a second sub-area, said first sub-area storing addresses of memory locations that are free, and said second sub-area storing read-sequence pointers.

11. (Original) The device according to claim 9 wherein said memory device further comprises a digital flash EEPROM of the multilevel type.

12-14. (Canceled)

15. (Previously Presented) An electronic device for the recording/reproduction of voice data, comprising:

a chip of semiconductor material;

a main transmission line integrated in said chip;

a control unit integrated in said chip and coupled to said main transmission line, the control unit being structured to provide a user interface to a user via an external user interface device;

a signal-conversion unit integrated in said chip and coupled to said main transmission line, said signal-conversion unit receiving an input analog signal correlated to an analog voice signal and including:

a converter circuit coupled to receive said input analog signal and operating a compression/decompression algorithm that compresses said input analog signal and generates a first stream of compressed digital signals, and decompresses a second stream of compressed digital signals and generates an output analog signal, and

first and second memory buffers coupled to said main transmission line and coupled to said converter circuit to sequentially receive said first and second streams of compressed digital signals;

a non-volatile memory unit integrated in said chip and coupled to said main transmission line, said non-volatile memory unit storing said first stream of compressed digital signals in memory locations, and generating said second stream of compressed digital signals according to first control signals generated by said control unit; and

a memory unit interface integrated in said chip and coupled between the non-volatile memory unit and said main transmission line, the memory unit interface being structured to coordinate exchange of data and instructions between the non-volatile memory unit and said main transmission line.

16. (Original) The device according to claim 15 wherein said converter circuit further operates an algorithm that generates blocks of digital signals having a predetermined dimension.

17. (Original) The device according to claim 16 wherein said signal-conversion unit further comprises a control circuit, said control circuit controlling transfer of said blocks of digital signals alternately to said first memory buffer and said second memory buffer according to second control signals supplied by said control unit.

18. (Original) The device according to claim 17 wherein said first and second memory buffers each further comprise RAM-type memory buffers.

19. (Original) The device according to claim 17 wherein said control circuit further comprises:

transferring means for transferring first blocks of digital signals to said first memory buffer;

first detecting means for detecting filling of said first memory buffer;

first transfer-switching means for transferring second blocks of digital signals to said second memory buffer and for sending said first blocks of digital signals to said non-volatile memory unit;

second detecting means for detecting filling of said second memory buffer; and

second transfer-switching means for transferring third blocks of digital signals to said first memory buffer and for sending said second blocks of digital signals to said non-volatile memory unit.

20. (Original) The device according to claim 15 wherein said non-volatile memory unit further comprises:

a first memory area storing said first stream of digital signals in said memory locations; and

a second memory area storing information regarding occupation of said memory locations of said first memory area.

21. (Original) The device according to claim 20 wherein said second memory area further comprises a first sub-area and a second sub-area, said first sub-area having addresses of unfilled memory locations stored therein, and said second sub-area having read-sequence pointers stored therein.

22. (Original) The device according to claim 20 wherein said memory device further comprises a digital flash EEPROM of the multilevel type.

23-25. (Canceled)